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FN-439
2100.001
7000.687

High Speed Video Data Acquisition System (VDAS) for H.E.P., Including Reference Frame Subtractor, Data Compactor and 16 Megabyte FIFO*

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October 1986

*(Submitted to the 1986 IEEE Nuclear Science Symposium, Washington, D.C., October 29-31, 1986)

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Abstract

A Video-Data-Acquisition-System (VDAS) has been developed to record image data from a scintillating glass fiber-optic target developed for High Energy Physics[1],[2]. VDAS consists of a combination flash ADC, reference frame subtractor, high speed data compactor, an N megabyte First-In-First-Out (FIFO) memory (where N is a multiple of 4), and a single board computer as a control processor. System data rates are in excess of 30 megabytes/second. The reference frame subtractor in conjunction with the data compactor records only the differences from a standard frame. This greatly reduces the amount data needed to record an image. Typical image sizes are reduced by as much as a factor of 20. With the exception of the ECL ADC board, the system uses standard TTL components to minmize power consumption and cost. VDAS operation as well as enhancements to the original system are discussed.

Introduction

The Video-Data-Acquisition-System was initially developed to provide a solution to the problems of collecting and handling very large amounts of image data. The system was also intended as an alternative to high speed film cameras for recording high energy particle tracks in scintillating glass targets or bubble chambers. VDAS evolved along with scintillating glass targets as a part of Fermilab experiment E-687, which expects to record approximately four million particle interaction events.

The scintillating glass fiber-optic plate is used as an active target for vertex detection and identification of rare particle decays. The target produces an image which is a two-dimensional projection of the tracks caused by any ionizing particle which passes through it. The light from this image is at the single to few photon level and needs several stages of image intensification to be recorded. A video camera (either CCD or vidicon) is used to convert the projected image into a form that can be digitized and processed by VDAS. While VDAS has been used mostly for digitizing standard video signals, it is capable of handling video data at any rate up to 30 million pixels per second.

VDAS has several advantages over the use of film to record particle interactions. The speed advantage is obvious, although an even greater advantage is that image data is directly accessible via computer. There is no longer the need for chemical film processing or tedious manual image digitization. There is also no longer the need to store large volumes of film in controlled environments, and with the use of an opitcal disk storage system even the space necessary to store digital data is greatly reduced. While originally designed to replace film for recording HEP interactions, VDAS has found capabilities beyond those of film.

VDAS, while originally designed solely as a data acquisition system, has been expanded to increase its capabilities. In order to aid in the analysis of image data, VDAS has had several modifications. These include the addition of a hardware data de-compactor to augment the data compactor, and an image averager which greatly increases the speed of image reconstruction. With these additions VDAS has broadened its scope to include image analysis

General System Overview/Operation

The major subsystems of VDAS for HEP are shown in Figure 1. These include; a combination flash ADC, reference frame subtractor and high speed data compactor board, a number of 4 megabyte FIFO memory modules, a control and display processor, and an optical disk drive. Additional systems have been developed which supplement this basic configuration.

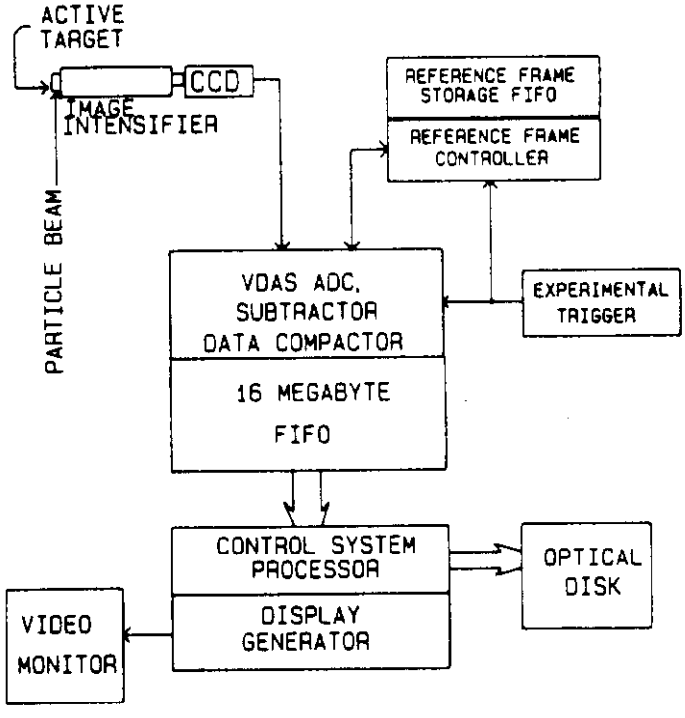

Figure 1. Overall block diagram of VDAS showing use of system as readout for scintillating glass active target.

*Operated by Universities Research Association Inc., under a contract with the United States Department of Energy.

These include a hardware data de-compactor and and an image averager. The control and display system contains commercially available hardware, two single board computers, one parallel I/O card, and a video display generator.

The video signal to be processed enters the ADC/Compactor board where it is flash converted to digital data with 6 bits of resolution. This 6 bit data word is processed by the data compactor to form an 8 bit byte [3]. These bytes are assembled into a 32 bit word which is then relayed to the FIFO memory. The FIFO is used as a high speed buffer to store bursts of image data from the compactor. The control processor is used to move data from the FIFO onto the optical disk for permanent storage or into a video display generator for viewing.

Analog to Digital Converter/Compactor Board

The ADC/Compactor system is a high speed image acquisition system. This system is the heart of VDAS and has the highest speed components. It consists of two seperate circuit boards, a Trigger and Sync board implemented in TTL and the ADC/Compactor board, which is primarily ECL.

The Trigger and Sync board performs the function of keeping the camera and the ADC/Compactor in locked step. It also accepts the experimental trigger, and can source or accept horizontal and vertical sync pulses. This board has a programable image size up to a maximum of 4096 by 4096 pixels and can operate at a pixel rate of up to of 30 MHz. The board was designed to be as flexible as possible to allow a variety of cameras to be used.

The Sync board contains circuitry which writes the following information into the data stream during the vertical interval of an image, a 24-bit frame count, a 24-bit byte count, a 24-bit experimental trigger identification number, a status word that contains the 6-bit compaction threshold in use at the time, and finally a 24-bit run number. This vertical sync information should allow the image data to be correlated with the tracking spectrometer data for the four million interactions recorded in the experiment.

The ADC/Compactor board, shown in Figure 2, performs the task of converting the video signal to digital form. It also contains the data compactor and the reference frame subtractor. The ADC section uses either a Siemens 6020 or 5200 flash ADC to produce 6 bits of data corresponding to 64 levels of intensity or grey scale. These intensity values will be used to measure the track of a particle to a greater degree of accuracy than is inherent in the resolution of the camera.

The converted image data is passed to the reference frame subtractor where it is digitally subtracted from the reference image. Only the differences between the two images are passed on to the compactor. The data compactor operates on the difference data, compressing it to reduce the amount of storage needed to reconstruct the image.

Compacting the data allows more images/second to be recorded, since the limiting factor in the data stream is the speed of the mass storage device. By reducing the number of bytes/image, the number of images is increased. The compaction method causes no degradation of image information, since the loss of image resolution would make the task of reconstructing the physics of the interaction much more difficult.

The ADC/Compactor board contains circuitry which packs the data into 32 bit words. These words are converted to TTL and are passed to the FIFO.

Sixteen Megabyte FIFO

The First-In-First-Out memory for use in the High Energy Physics application was designed to be an inexpensive, expandable, and fast buffer. A working prototype of an eight megabyte FIFO, shown in Figure 3, was constructed. The prototype met the cost and speed requirements and proved the techniques used in the FIFO design, but was not easily expandable.

Keeping system costs low and expandability high was achieved by making a basic FIFO module 4 megabytes in size. This allowed printed circuit boards to be manufactured that were of a reasonable physical size.

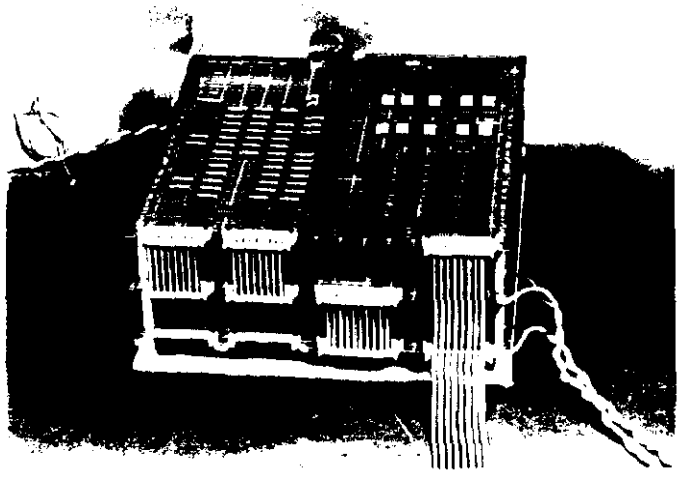

Figure 2. Photograph of prototype VDAS ADC/Compactor Board.

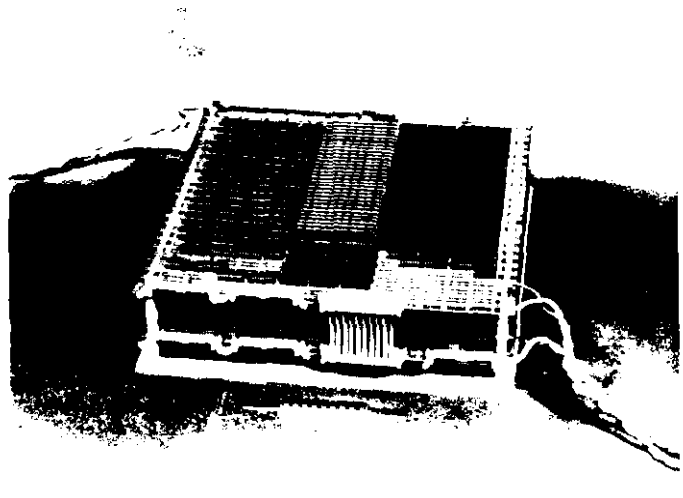

Figure 3. Photograph of prototype eight megabyte FIFO memory array.

A basic FIFO would now consist of a single controller board and anywhere from 1 to 64, 4 megabyte memory modules. This design change allowed large FIFOs to be easily assembled, ranging in memory capacity from 4 megabytes, to a maximum of 256 megabytes.

Each FIFO memory module consists of 18 NMOS 256K x 9 DRAM SIP modules, choosen for low cost, low power consumption, and ease of replacement. The FIFO uses ALS/AS TTL for input/output shift registers, storage registers, and all FIFO control circuitry. These components achive the desired speed with lower levels of power consumption than could be achieved using ECL components.

The FIFO attains its speed by incorporating a parallel architecture which allows the use of low power, low speed components. For example, the 18 megabyte FIFO which will be used for HEP contains 4 memory modules and a controller. Externally, this FIFO appears as a buffer 32 bits wide and 4 megawords deep. Internally, however, the FIFO is organized as 262,144 words 512 bits long. Details of the FIFO's parallel architecture are discussed in a previous paper [3].

A consequence of this FIFO architecture is that the larger the number of FIFO memory modules in the system, the faster the data rates through the FIFO can be. The 18 megabyte FIFO can, in principle, handle input data rates of up to 140 megabytes/sec. At this time, however, no attempt has been made to exceed 30 megabytes/sec. The final limiting factor in the data rates through the FIFO is the input and output shift registers which should be able to run at at least 50 MHz which is a data rate of 200 megabytes/second.

VDAS Enhancements

Hardware Data De-packer

Designed for High Energy Physics, VDAS has already found uses elsewhere. VDAS with minor additions was recently used to record images of Comet Halley [4]. The Hardware Data De-packer evolved from the need to reconstruct images at a higher rate than was being accomplished by offline software.

Software Image Reconstruction

In software image reconstruction, data would be read out of the FIFO via an 8-bit parallel I/O port. Each byte was examined to determine its identity, whether image data, zero count, horizontal or vertical sync. Image data, when found, would be written into the video display generator. Zero counts were handled differently, the identifying bit was removed and the remainder of the byte was used as a count for the number of zeros which must be loaded into the display generator. Horizontal and vertical sync bytes, when identified, were used to reset the line pointers in the video display generator.

Analysis of the software image reconstruction revealed that a substantial amount of the processing time was consumed by bit manipulations used to identify the different image data types. The problem of increasing image reconstruction speed did not appear to have an easy solution. Various proposals were considered as a solution to this problem. Faster and larger processors with more memory and better data handling capabilities were considered. While these processors would increase the speed of image reconstruction, the increase would be at best a factor of 2 or 3. This solution would also have forced the rewriting of the control systems software. There was an additional demand placed on any solution that it be done quickly, as the Comet Halley observations could not be delayed. Rewriting the total system software was deemed too long a task to make this a viable solution.

A hardware data de-packer seemed to be the best solution. It would allow the use of the existing control processor and would require only minimal rewriting of the software. The hardware de-packer takes advantage of the fact that the data compaction scheme produces data which is self identifing. This data encryption scheme lends itself easily to hardware de-compaction. A circuit to perform this function was quickly constructed as it required few components. The de-packer operates by reading data out of the FIFO performing the de-compaction and recreating the data stream as it appeared prior to compaction. This data stream is then available for quick image reconstruction.

The hardware de-packer, shown in Figure 4, includes a set of 4, 8-bit latches to hold the 32-bit FIFO word. The data is strobed into these latches and a 2-bit ring counter selects the data byte to operate upon. The indentifier bits in the data activate different parts of the control circuitry. If the most significant bit is set, the byte is identifed as data or horizontal or vertical sync, and is passed directly through the system. As each byte is read from the board, the ring counter increments to select the next data word.

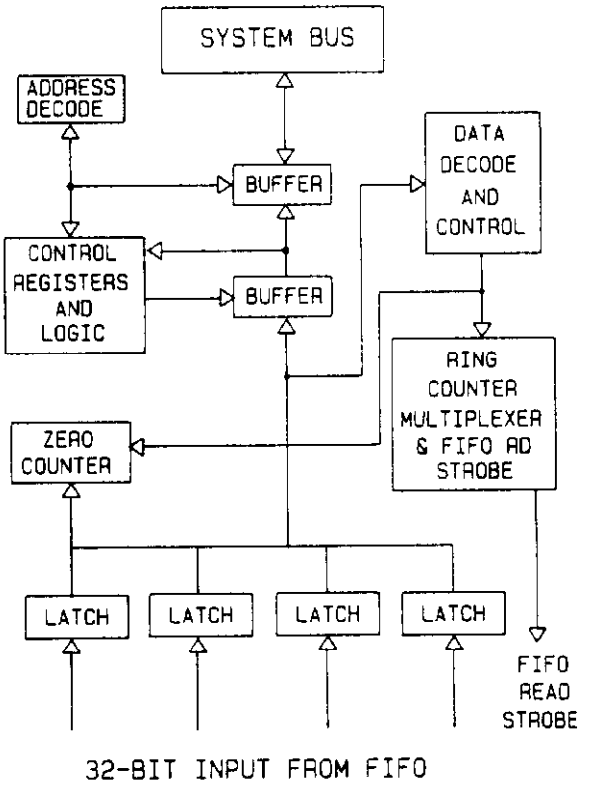

Figure 4. Block diagram of hardware data de-packer.

When a data word is detected with its MSB being reset, a zero count has been identified. The circuitry then initiates a different set of procedures; the zero count is loaded into an 8 bit down counter, and a register is cleared to force the proper data value (Hex 00 for a Null pixel) into the data stream. After every read from the data stream the zero counter is decremented until it reaches zero, at this point the ring counter is re-enabled and the de-packer resumes normal operation.

While doubling the processor speed would have gained only a factor of 2 in image reconstruction, the use of the hardware de-packer gained an immediate factor of 3 in reconstruction speed. Although the de-packer had removed the task of image reconstruction from the processor, the processor was still saddled with the time consuming task of image averaging.

Hardware Image Averager

Image averaging was needed for the comet observations to reduce noise caused by the image intensifiers. One of the requirements of image averaging is to have a memory of adequate size to hold an entire image. This memory must have a sufficient word length to allow multiple additions without causing an overflow.

Given enough memory, image averaging could be performed in software. However, the speed would not be acceptable for this application. Following the success of implimenting the de-packer in hardware, it was decided to design a hardware image averager to increase image processing speed.

A hardware image averager which contained enough memory to store a de-compacted image was quickly designed and built, as was circuitry to perform the image addition and division.

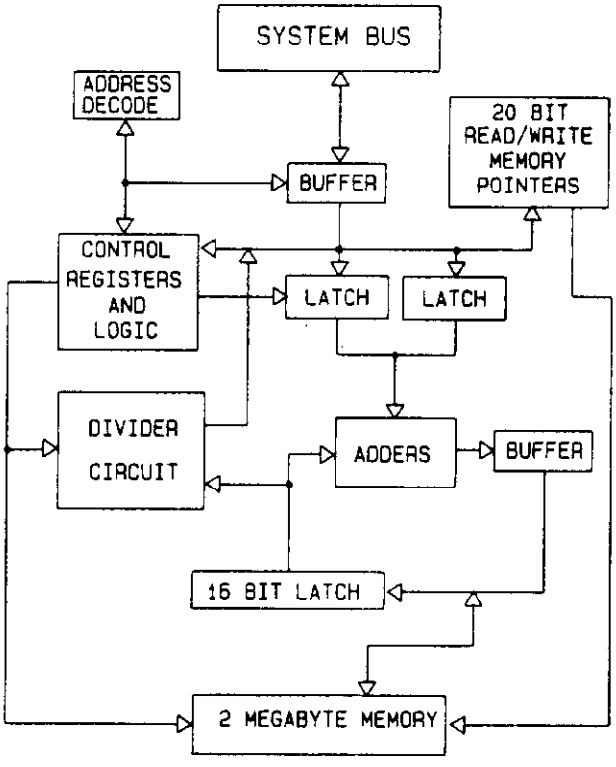

Figure 5. Block diagram of hardware image averager.

The block diagram of the image averager is shown in Figure 5. It consists of address decoding circuitry, control logic, read/writable memory pointers, adders, division circuit, and two megabytes of dynamic ram organized as 1 megaword. This memory size allows images as large as 1024 by 1024 to be averaged. By making the memory 16 bits wide the averager could hold the sum for 1024, 6-bit images. The averager functions automatically with parameters set by the control processor. Frames are simply transfered to the averager and are automatically added to the image sum. After the desired number of frames have been written to the averager, the "averaged" frame can be read out. This averaged frame is produced automatically upon readout from the image sum by a binary bit shift operation performed in hardware. This leaves the average memory unaltered so that it may be accessed again for other images. The data is divided by 1, 2, 4, 8, etc depending upon control parameters. The averager also contains a hardware self clear to zero the full 2 megabytes without processor intervention.

Reference Frame Subtractor

A reference frame subtractor is under design in order to more fully utilize the capabilities of the compactor and to keep the dynamic range of the imaging system as high as possible. The reference frame subtractor is capable of operating at over 30 megapixels per second. The subtractor consists of another 4 megabyte FIFO and a reference frame controller. The FIFO acts as the fast storage media for the image data which makes up the reference frame, it passes data to the reference controller which reformats the data and passes it to the subtractor. The reference controller uses the video sync signals to keep the reference frame and the current frame in step so that the individual pixels being recorded have the correct reference data subtracted. The subtractor is able to perform a "frame minus zero", which is no subtraction; "frame minus reference", which is the standard for a dark field with bright areas of interest; and "reference minus frame", which is useful for light backgrounds with dark areas of interest. The subtractor can force a zero value for a negative number to ignore data that is darker than reference. This mode can be disabled so that the resultant data is the true difference between the reference frame and the new frame.

The "dark mode" subtractor is used for scintillating glass target work where the subtractor eliminates the fixed pattern noise from the camera. The "light mode" subtractor could be used for bubble chambers where the tracks are darker than the background, this would allow the efficient compaction of images which are primarily bright and where only the differences from the standard frame are stored.

Results

High Energy Physics

The system has been used extensively for testing the optium combination of materials in scintillating glass targets. While the beamlines at Fermilab are shutdown for construction of upgrades to the accelerator, cosmic rays are used for target testing. A cosmic-ray telescope was used to produce a trigger which gated the image intensifier and digitizing system.

Images were first reconstructed using only the original software. These were then compared with the images which the hardware had reconstructed to verify de-packer and averager operation. Once these were fully checked the system could be run at a much higher rate using only the hardware with CPU supervision. The system was then used to examine the differences in various fiber-optic plate targets. Many tracks were observed in several targets in an effort to determine the optimum target configuration. Target parameters under consideration were fiber size, glass composition, cladding composition, and fiber length [4]. Targets were evaluated on the basis of the number of photons/mm which a minimum ionizing particle produced.

The FIFO has the capability to store at least 2000 frames of compacted data. The size of the FIFO is dictated by a combination of the beam spill structure used for the experiment and the speed with which data can be written to mass storage. The size needed for E-687 is estimated to be 16 megabytes.

Comet Halley

The Video-Data-Acquisition-System has found an application in astronomical observations. Most recently the system was used to study Comet Halley. Inserting a telescope in place of the scintillating glass fiber-optic plate provided the opportunity to do fast time resolution imaging of the comet. This has generated much interest in the system from the astronomical community. Preliminary results of the cometary observations are reported in a separate paper [5].

Conclusions

VDAS has performed as designed for High Energy Physics and should provide a more direct route for the analysis of particle interactions. With modifications, VDAS has been able to aid in image analysis as well as acquisition. The data acquisition capabilities and analysis features have been used to study Comet Halley in a unique way. It is hoped that VDAS may also find uses in other areas outside H.E.P. and astronomy.

References

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